16.8 A Back-Illuminated High-Sensitivity Small-Pixel Color CMOS Image Sensor with Flexible Layout of Metal Wiring

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The number of image sensors being produced, such as those used in video camcorders, digital still cameras, and cellular phone cameras is increasing every year. CCDs still dominate the market, especially in digital still cameras (DSC), which constitute the largest single application and for which there is pressure to reduce the pixel size. CCDs are currently ahead of CMOS image sensors (CIS) in terms of pixel size reduction [1]. The main reason that CCDs dominate the market is the lower image quality output of CIS devices, despite the fact that they offer many advantages such as high-speed operation and lower power consumption. One of the main reasons for this lower image quality is the lower sensitivity of the CIS device. The lower sensitivity is a result of the complicated structure above the photo-diode itself. Ordinary CIS devices use two or more metal layers, which act as an obstacle above the photo-diode. These metal layers obscure the light and reduce the photon gathering efficiency.

We set out to solve these problems and, in this study, developed a CIS device with metal wiring under the photo-diode, which is called a back-illuminated CIS. The structure above the photo-diode of this CIS is simple, consisting only of a color filter and an on-chip lens. There are no obstacles in the photon gathering path. We have incorporated this design into a 1/3.2inch, 1.3M-pixel CIS with 3.45μm square, three-transistor pixels. Figure 16.8.1 compares the cross-sections of our CIS with a conventional CIS. We confirmed that a back-illuminated structure offers advantages in terms of sensitivity and optical angle response. With our CIS, we can make the pixel size smaller and capture color images because we use an on-chip color filter, and do not use 3D interconnect in the pixels. Furthermore, the dark current is reduced with our device because we form the photo-diode and all of the circuits on the same silicon wafer [2, 3, 4].

In addition to the improvement in the photon gathering, the silicon thickness also affects the sensitivity. Figure 16.8.2 shows that our CIS with 4μm thick silicon has 38% higher sensitivity than a conventional CIS for parallel light at a wavelength of 540nm. The dependence of the sensitivity on silicon thickness at a wavelength of 540nm indicates that the sensitivity is saturated for 5μm-thick Silicon (i.e., there is almost 100% photon absorption). However, the photo-diode with a silicon thickness of 4μm has sufficient sensitivity for many applications. We went on to find that the degradation in the sensitivity is only slightly dependent on the angle at which the light enters the back-illuminated CIS. Figure 16.8.3 shows that, for our CIS, the degradation is only 20% at a 20° angle of incidence while the degradation is 85% for a conventional CIS at the same angle.

Figure 16.8.4 provides a table comparing the performance of our CIS to a conventional structure. The back-illuminated CIS offers improved sensitivity and *F*-number dependence. In addition to these improvements, the image lag and dark output are similar to those of a conventional CIS. Image lag results from poor charge transfer from the photo-diode to the floating diffusion through the read-out gate. No such image lag was observed with the test device, because a good potential profile was achieved in spite of the back-illuminated structure. The read-out transistors work well in spite of the light coming from the photo-diode side because a sufficient fraction of the photons are converted to electrons in the photo-diode. Figure 16.8.5 shows a high-sensitivity, low-noise color image without optical shading.

The back-illuminated CIS design is not only advantageous in terms of its optical characteristics, but also offers flexibility in terms of the metal wiring on the pixel area. With conventional front-illuminated devices, metal layers cannot be formed over the photo-diode because they would impede photon gathering. But, this rule can be safely ignored in the case of a back-illuminated device, because the metal wiring layers are actually under the photo-diode. This means that we have much more freedom in placing the metal wiring layers. In Figure 16.8.6, we propose an example cell layout with 2.5 transistors per pixel. This layout improves the other device characteristics relative to a conventional CIS, such as the saturation output, by enlarging the capacitance of the P-N junction of the photo-diode on the front face where the transistors exist. The photo-diode area of our CIS constitutes more than 50% of each pixel, while the value for a conventional CIS is less than 40%. Furthermore, for a conventional CIS, the asymmetric layout that is used to increase the front photo-diode area of shared pixels leads to a difference between the pixel optical center and the layout center. In our CIS, this difference does not affect the optical response because there are no metal layers above the photo-diode.

In conclusion, a small-pixel -3.45μm square pixel image sensor with 1.3M pixels in the 1/3.2inch format has been fabricated and tested. We confirmed that the device offers higher sensitivity and better performance in optical shading without any degradation in the device performance. This back-illuminated color CMOS image sensor is ideally suited to applications requiring high picture quality from a small pixel size.

Acknowledgments:
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References:
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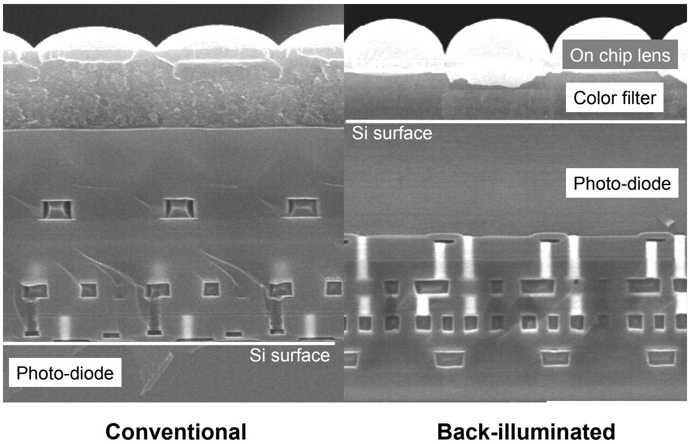

Figure 16.8.1: Cross section of CIS pixels.

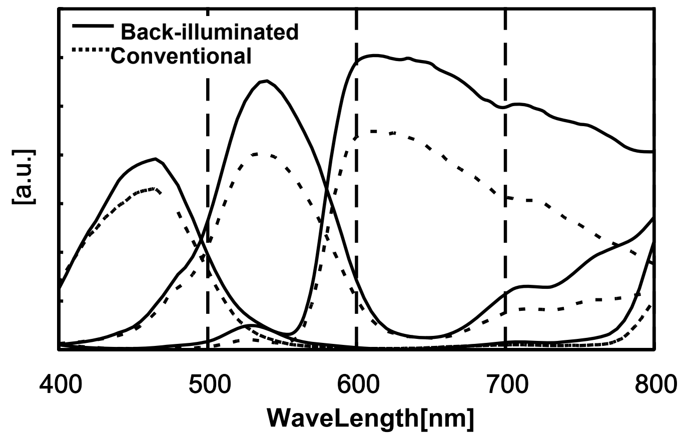

Figure 16.8.2: Measured spectrum.

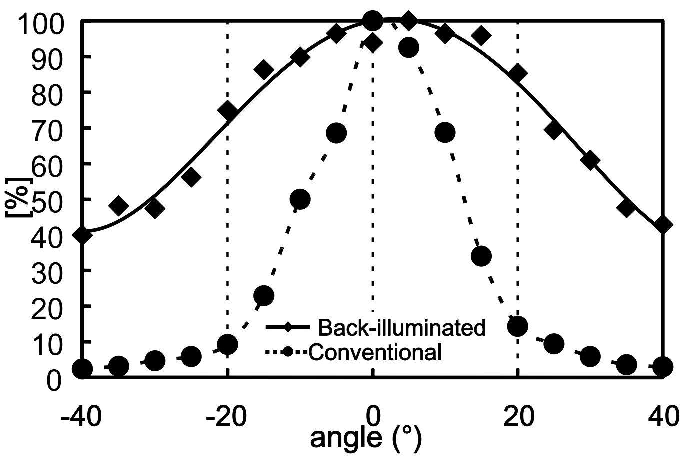

Figure 16.8.3: Measured optical angle response.

	Back-illuminated	Conventional
Process	0.25µm 1Poly/3Metal	
Optical format	1/3.2 inch	
Number of pixels	1296 x 985	
Supply voltage	2.7V (analog) / 1.8V (digital)	
Frame rate	15 frame /sec	
Read out Freq.	24MHz	
Saturation output	1020mV	1028mV
Sensitivity	276mV	200mV
F num. dependency (F2.8/5.6)	0.99	0.86
Image lag	1.64mV	1.38mV
Dark output	1.23mV	1.00mV

Figure 16.8.4: Performance comparison.

Figure 16.8.5: Captured image.

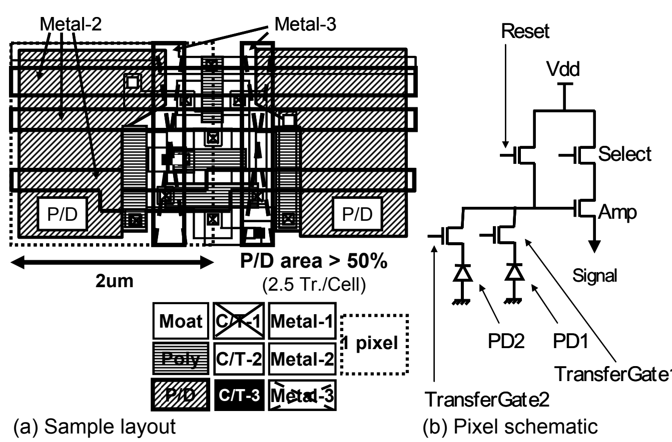

Figure 16.8.6: Sample layout and pixel schematic.